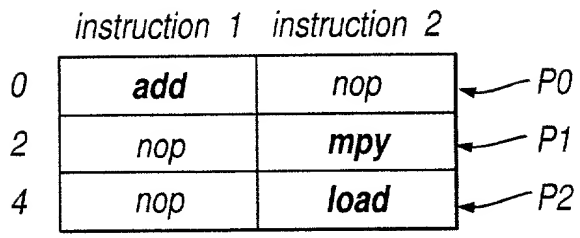


Fig.1(A)

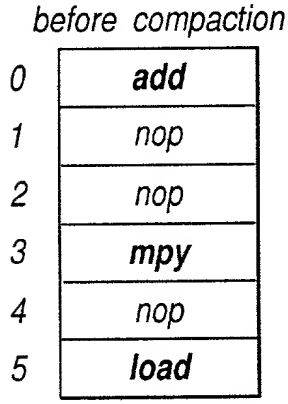


Fig.1(B)

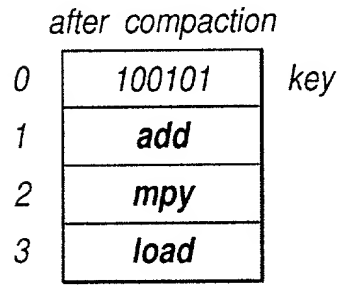


Fig.1(C)

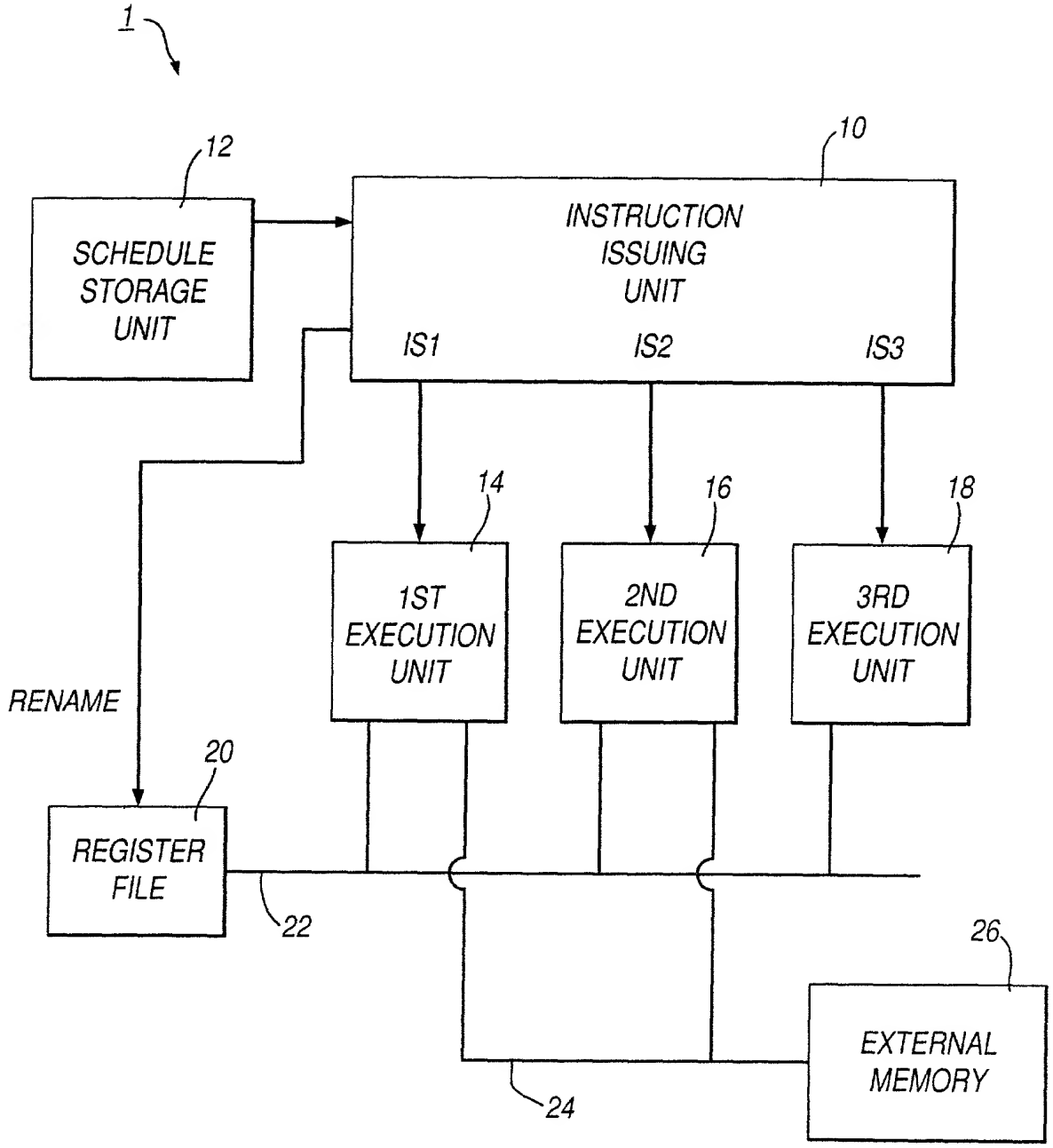

1
12
10
SCHEDULE STORAGE UNIT
INSTRUCTION ISSUING UNIT
IS1
IS2
IS3
14
16
18
1ST EXECUTION UNIT
2ND EXECUTION UNIT
3RD EXECUTION UNIT
RENAME
20
REGISTER FILE
22
26
EXTERNAL MEMORY
24

Fig.2

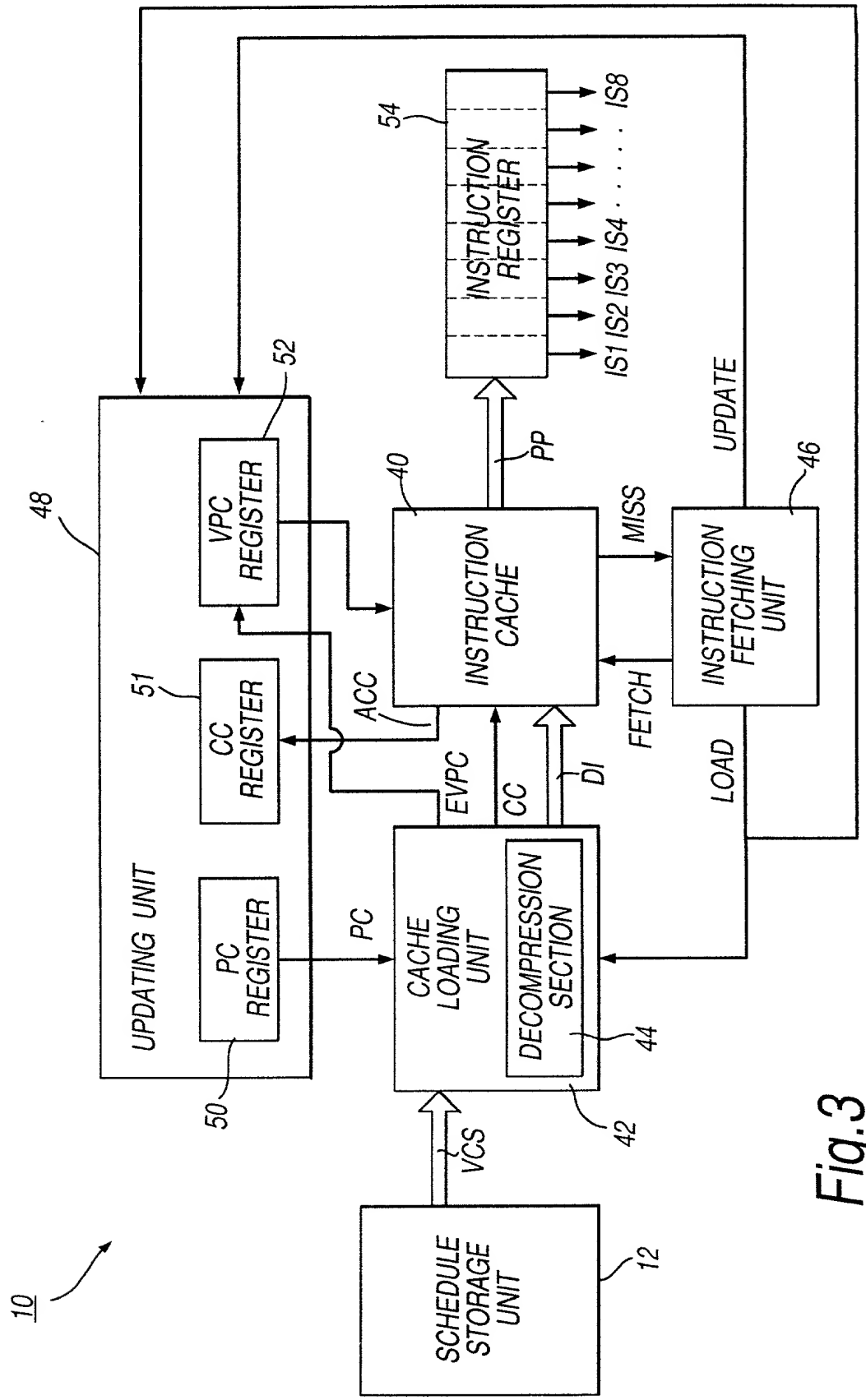

10
SCHEDULE STORAGE UNIT
12
VCS
CACHE LOADING UNIT
DECOMPRESSION SECTION
42
44
PC
PC REGISTER
50
UPDATING UNIT
48
CC REGISTER
51
VPC REGISTER
52
ACC
EVPC
CC
DI
INSTRUCTION CACHE
40
PP
INSTRUCTION REGISTER
54
IS1 IS2 IS3 IS4 . . . . IS8
MISS
FETCH
INSTRUCTION FETCHING UNIT
46
LOAD
UPDATE

Fig.3

4/13

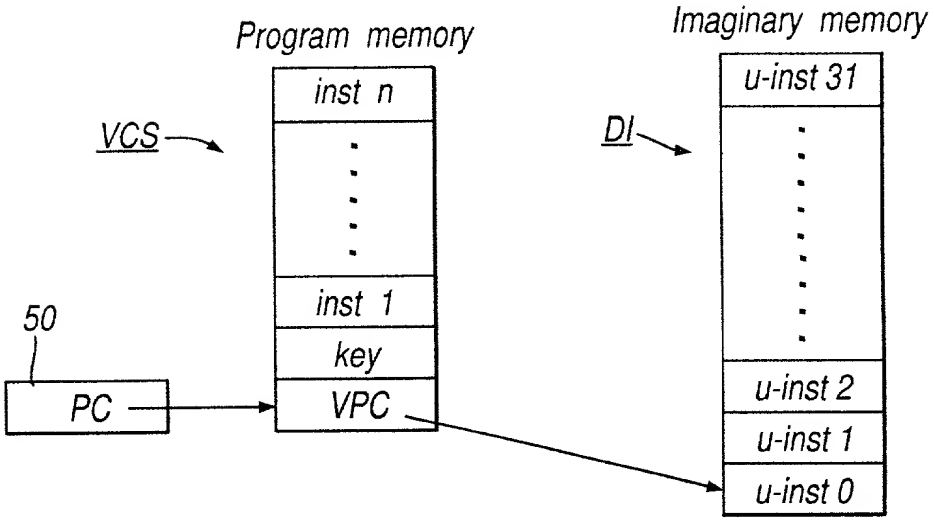


Fig.4

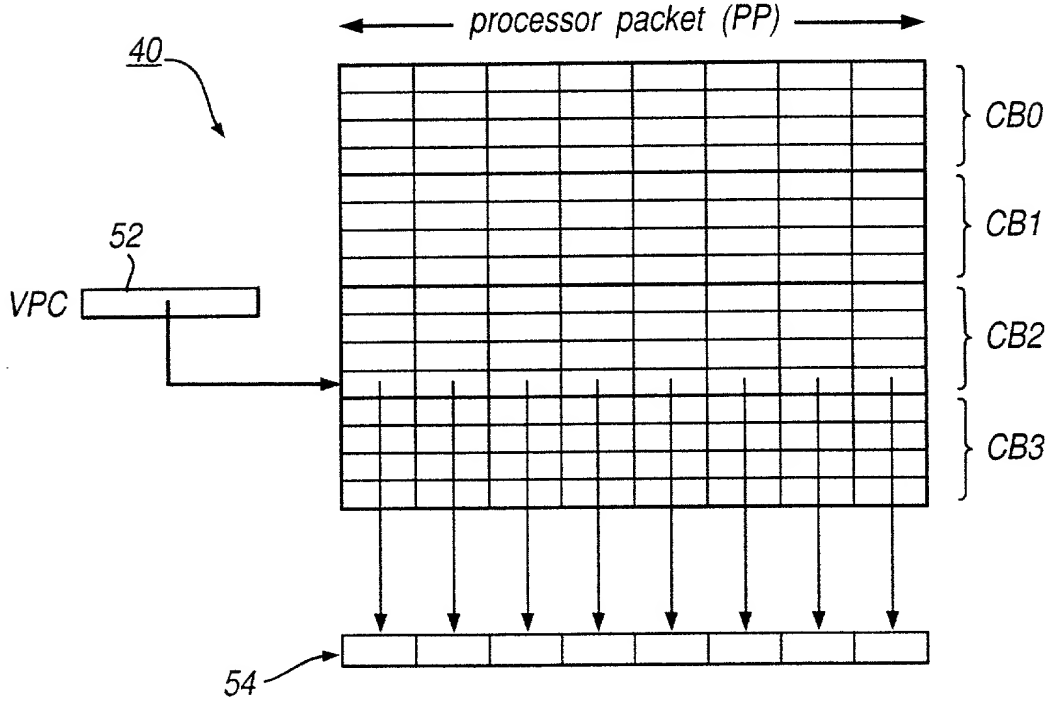


Fig.5

5/13

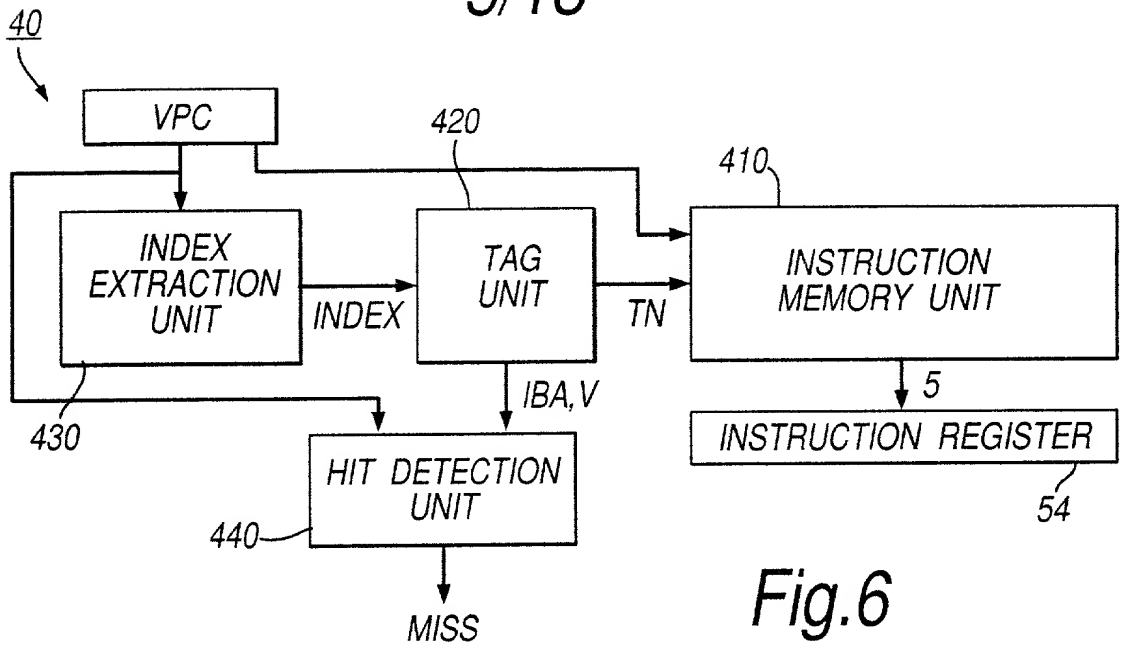


Fig.6

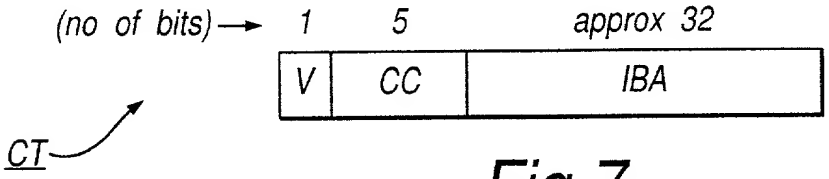


Fig.7

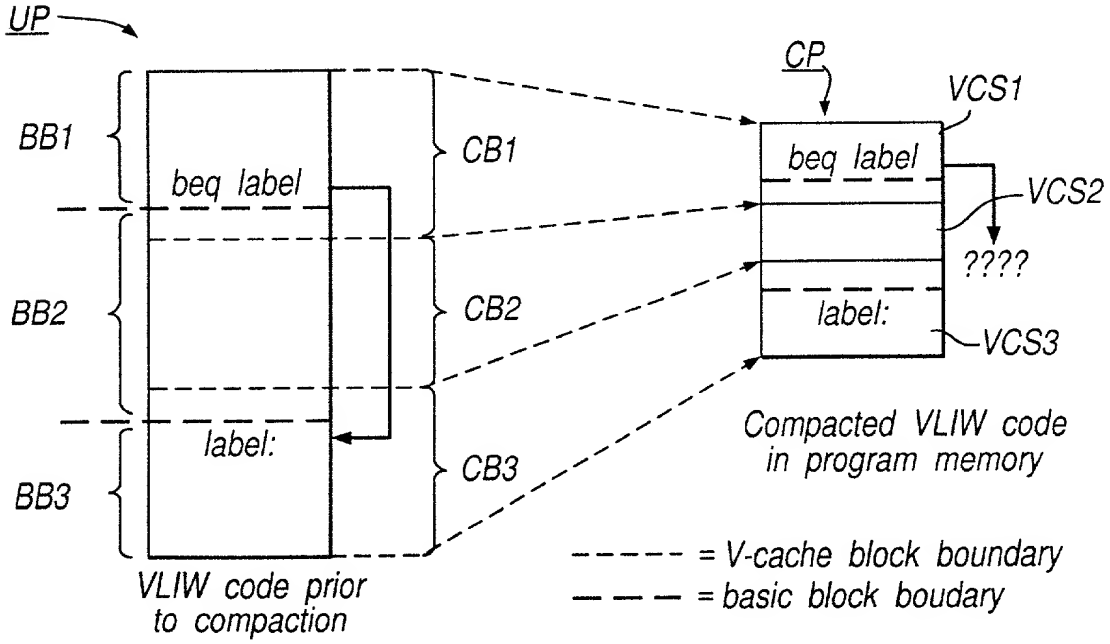


Fig.9

6/13

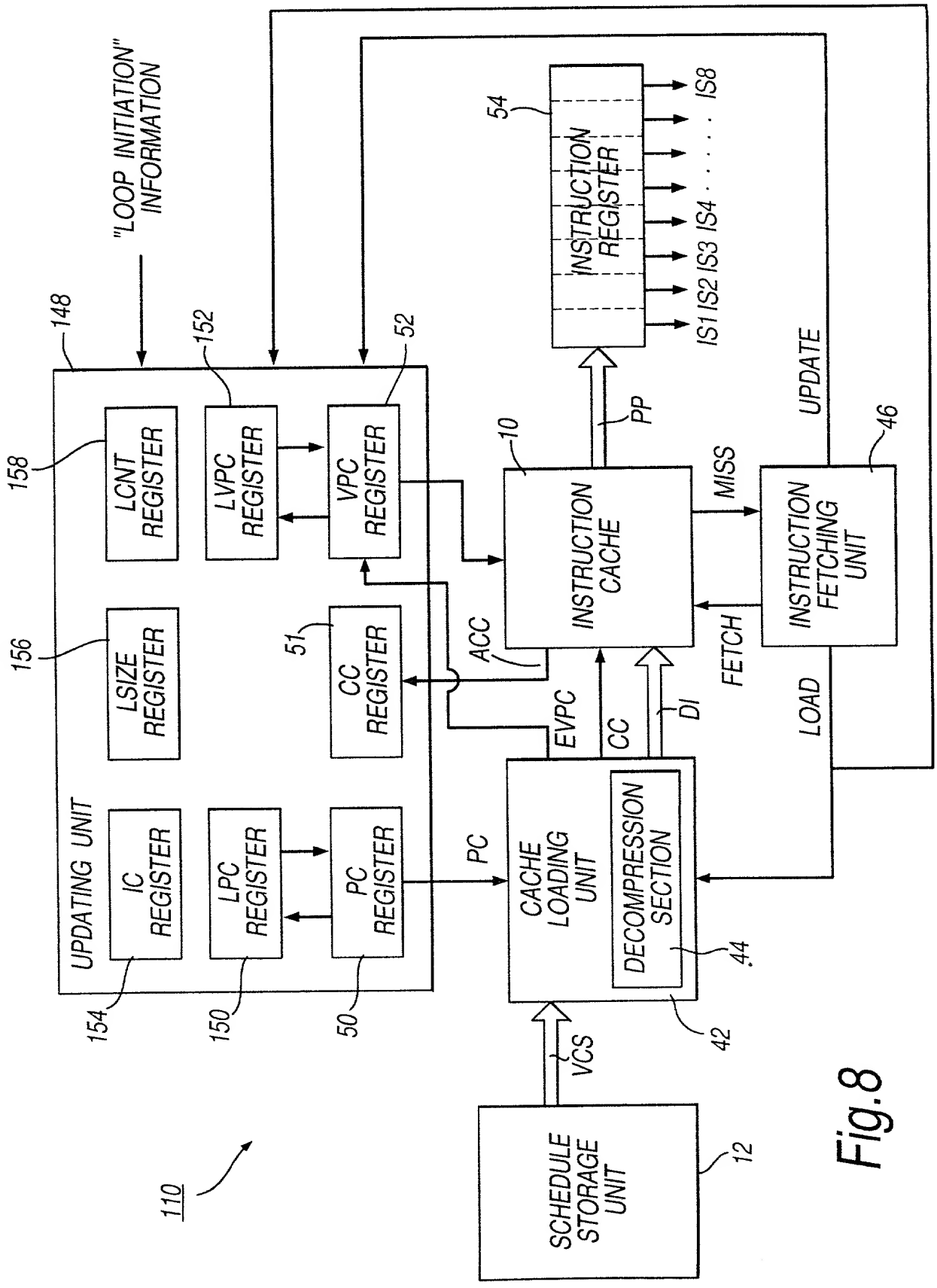

"LOOP INITIATION" INFORMATION
148
152
52
54
INSTRUCTION REGISTER
IS1 IS2 IS3 IS4 . . . . IS8
158
LCNT REGISTER
LVPC REGISTER
VPC REGISTER
PP
10
UPDATE
46
MISS
INSTRUCTION CACHE
INSTRUCTION FETCHING UNIT
156
LSIZE REGISTER
51
CC REGISTER
ACC
FETCH
EVPC
CC
DI
LOAD
UPDATING UNIT
IC REGISTER
LPC REGISTER
PC REGISTER
PC
CACHE LOADING UNIT
DECOMPRESSION SECTION
44
154
150
50
42
VCS
SCHEDULE STORAGE UNIT
12
110

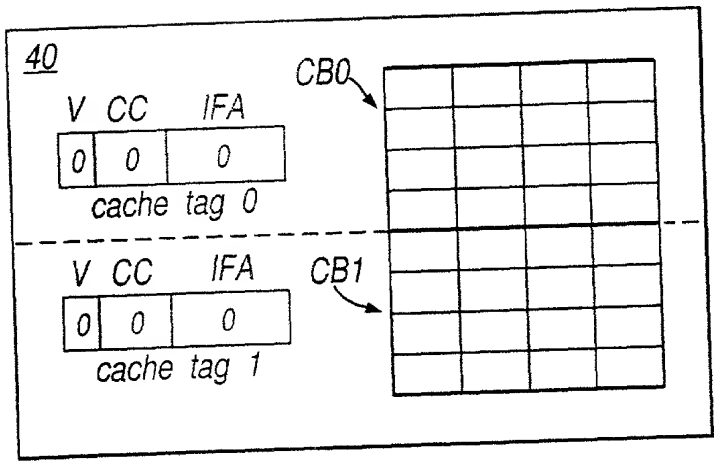
Fig.8

	-	I1	I2	-	1000
	loop 8, r1	-	-	-	1010
loop:	I3	I4	-	-	1020
	-	I5	-	I6	1030
	-	I7	-	-	1040
	I8	I9	-	-	1050
	-	I10	-	I11	1060
	-	-	-	I12	1070
	-	I13	I14	-	1080
	I15	-	I16	-	1090
	-	I17	-	I18	10a0
	I19	-	-	I20	10b0

Fig.10

VCS1	1000	2000
	key1	2004
	I1	2008
	I2	200c
	loop 8, r1	2010
	I3	2014
	I4	2018
	I5	201c
	I6	2020
VCS2	1040	2024
	key2	2028
	I7	202c
	I8	2030
	I9	2034
	I10	2038
	I11	203c
	I12	2040
VCS3	1080	2044
	key3	2048
	I13	204c
	I14	2050
	I15	2054
	I16	2058
	I17	205c
	I18	2060
	I19	2064
	I20	2068

Fig.11


40
V CC IFA
0 0 0
cache tag 0
CB0
V CC IFA
0 0 0
cache tag 1
CB1

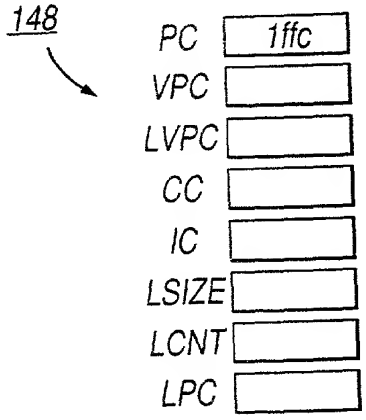
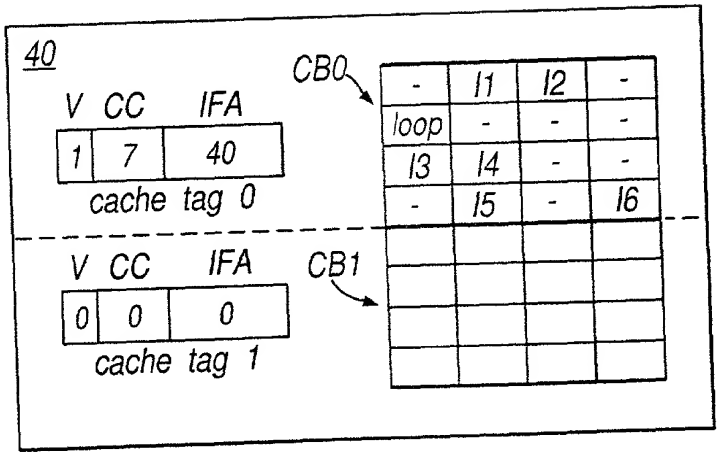

148
PC 1ffc
VPC
LVPC
CC
IC
LSIZE
LCNT
LPC

Fig.12


40
V CC IFA
1 7 40
cache tag 0
CB0
- I1 I2 -
loop - - -
I3 I4 - -
- I5 - I6
V CC IFA
0 0 0
cache tag 1
CB1

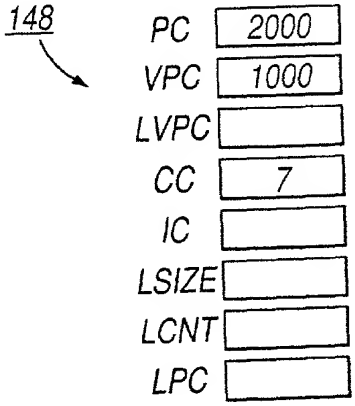
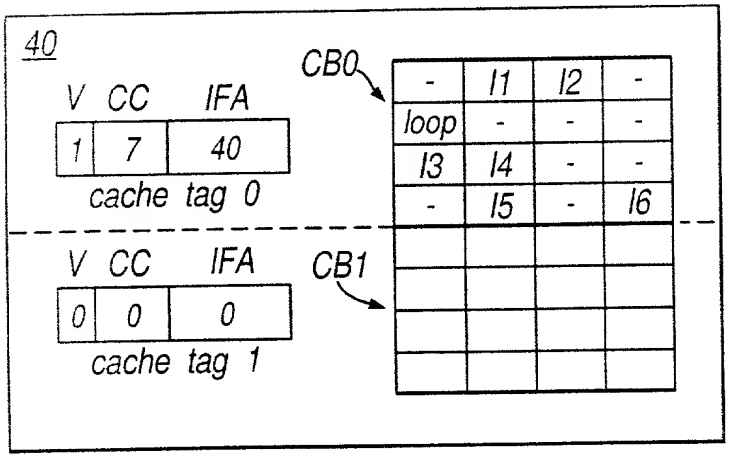

148
PC 2000
VPC 1000
LVPC
CC 7
IC
LSIZE
LCNT
LPC

Fig.13


40
V CC IFA
1 7 40
cache tag 0
V CC IFA
0 0 0
cache tag 1
CB0
CB1
- I1 I2 -
loop - - -
I3 I4 - -
- I5 - I6

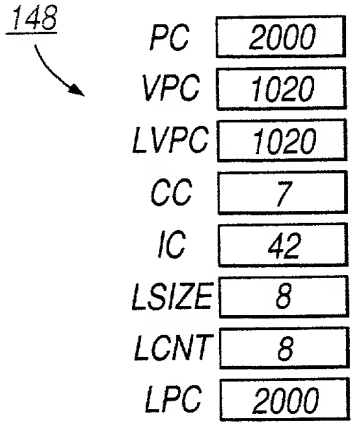
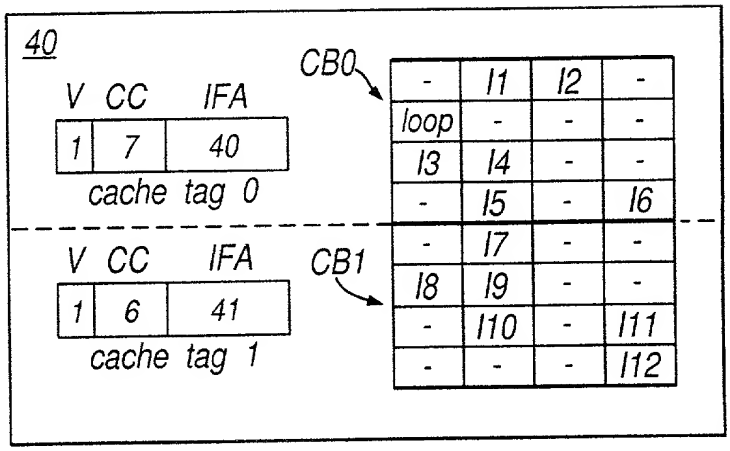

148
PC 2000
VPC 1020
LVPC 1020
CC 7
IC 42
LSIZE 8
LCNT 8
LPC 2000

Fig.14


40
V CC IFA
1 7 40
cache tag 0
V CC IFA
1 6 41
cache tag 1
CB0
CB1
- I1 I2 -
loop - - -
I3 I4 - -
- I5 - I6
- I7 - -
I8 I9 - -
- I10 - I11
- - - I12

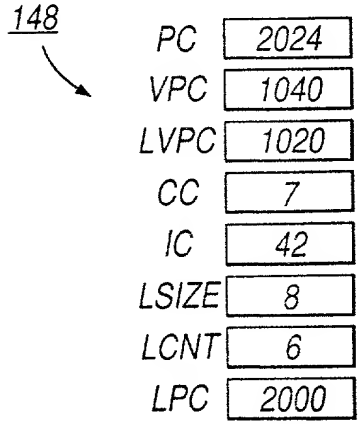
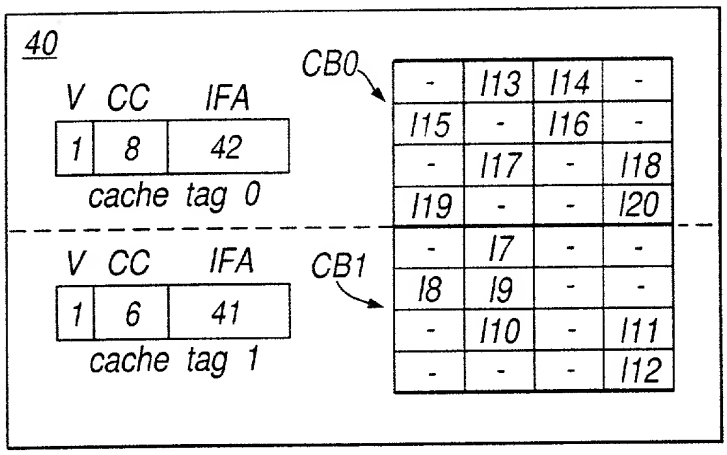

148
PC 2024
VPC 1040
LVPC 1020
CC 7
IC 42
LSIZE 8
LCNT 6
LPC 2000

Fig.15


40
V CC IFA
1 8 42
cache tag 0
V CC IFA
1 6 41
cache tag 1
CB0
- I13 I14 -
I15 - I16 -
- I17 - I18
I19 - - I20
CB1
- I7 - -
I8 I9 - -
- I10 - I11
- - - I12

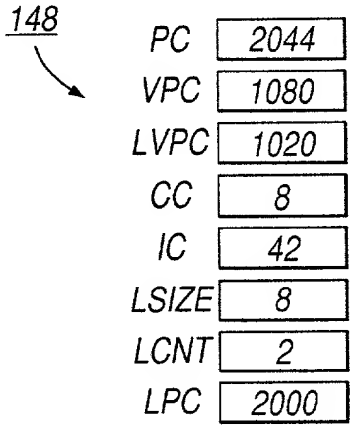
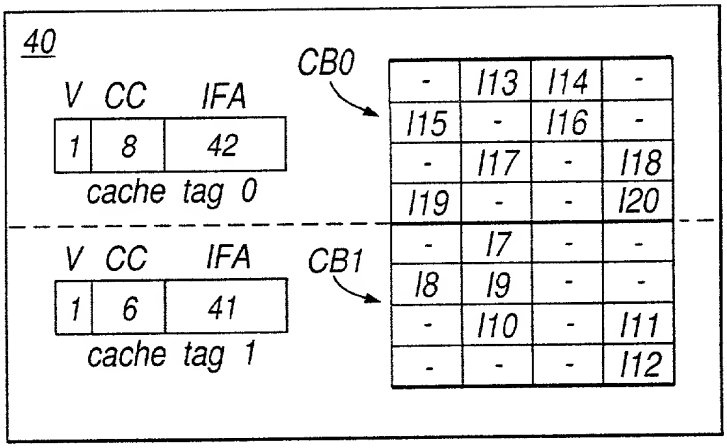

148
PC 2044
VPC 1080
LVPC 1020
CC 8
IC 42
LSIZE 8
LCNT 2
LPC 2000

Fig.16


40
V CC IFA
1 8 42
cache tag 0
V CC IFA
1 6 41
cache tag 1
CB0
- I13 I14 -
I15 - I16 -
- I17 - I18
I19 - - I20
CB1
- I7 - -
I8 I9 - -
- I10 - I11
- - - I12

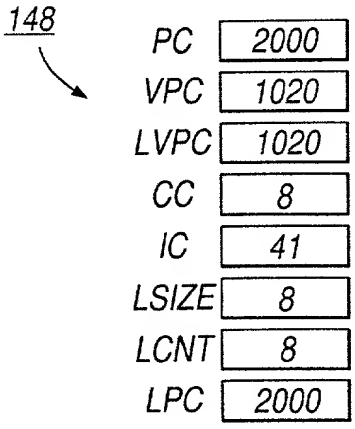
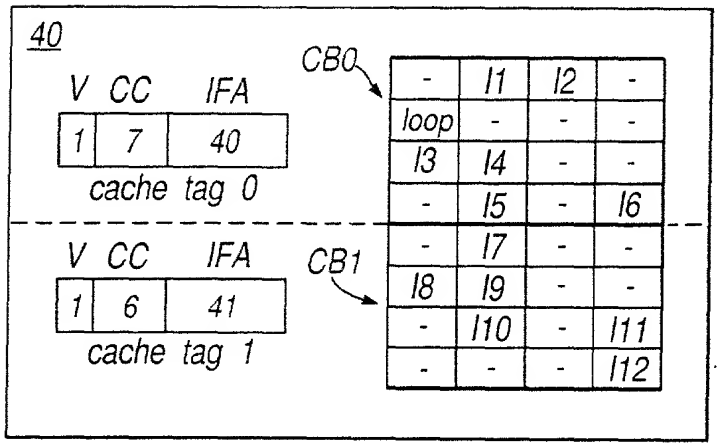

148
PC 2000
VPC 1020
LVPC 1020
CC 8
IC 41
LSIZE 8
LCNT 8
LPC 2000

Fig.17


40
V CC IFA
1 7 40
cache tag 0
V CC IFA
1 6 41
cache tag 1
CB0
CB1
- I1 I2 -
loop - - -
I3 I4 - -
- I5 - I6
- I7 - -
I8 I9 - -
- I10 - I11
- - - I12

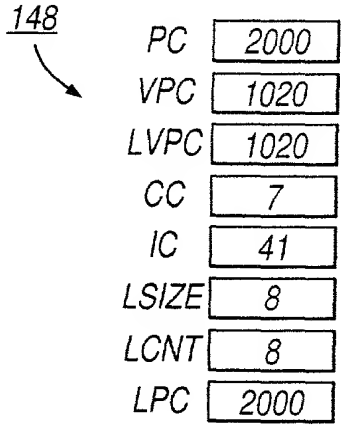
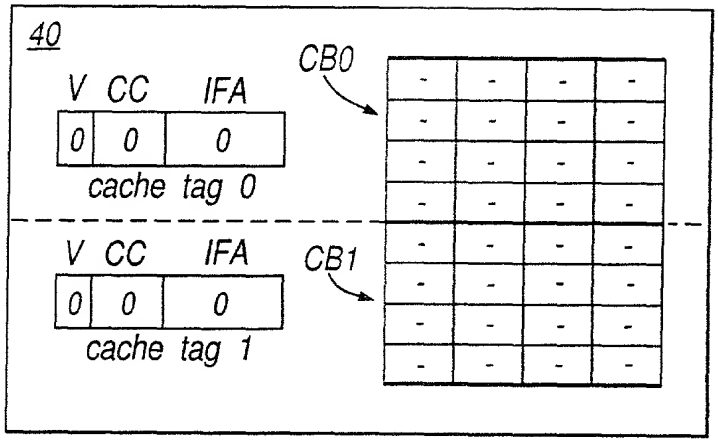

148
PC 2000
VPC 1020
LVPC 1020
CC 7
IC 41
LSIZE 8
LCNT 8
LPC 2000

Fig.18


40
V CC IFA
0 0 0
cache tag 0
V CC IFA
0 0 0
cache tag 1
CB0
CB1

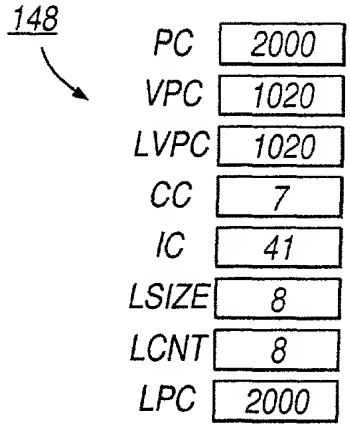

148
PC 2000
VPC 1020
LVPC 1020
CC 7
IC 41
LSIZE 8
LCNT 8
LPC 2000

Fig.19

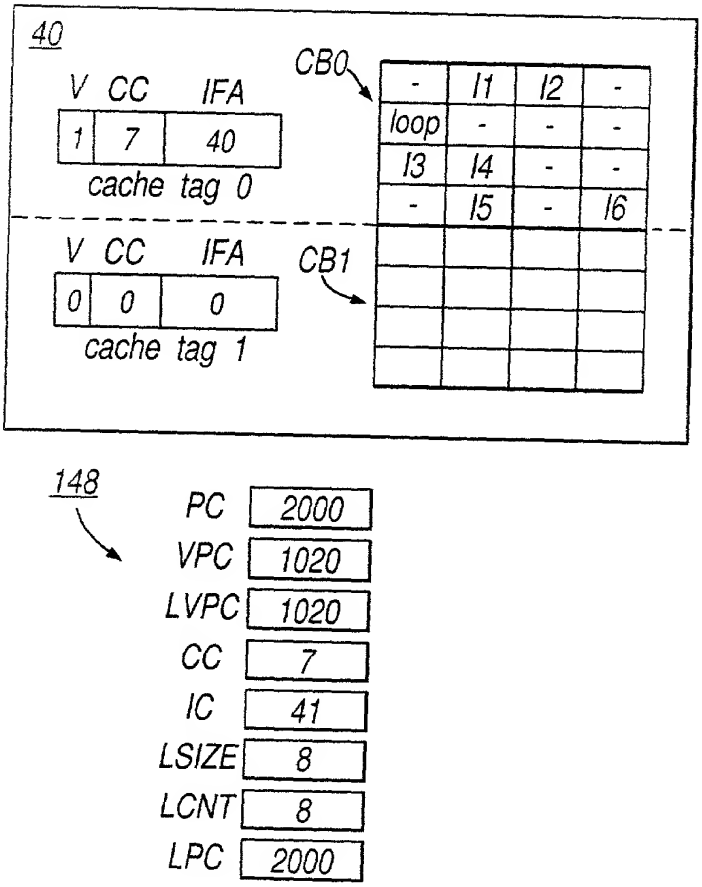


Fig.20

0808.65559

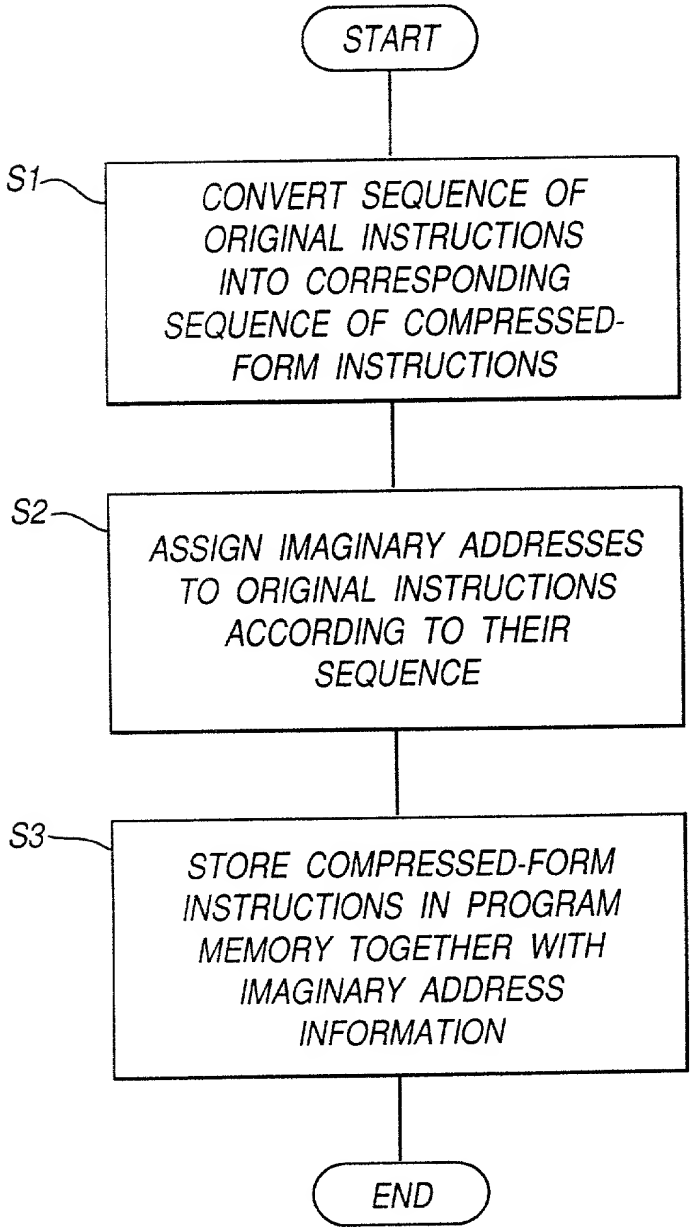

START
S1
CONVERT SEQUENCE OF ORIGINAL INSTRUCTIONS INTO CORRESPONDING SEQUENCE OF COMPRESSED-FORM INSTRUCTIONS
S2
ASSIGN IMAGINARY ADDRESSES TO ORIGINAL INSTRUCTIONS ACCORDING TO THEIR SEQUENCE
S3
STORE COMPRESSED-FORM INSTRUCTIONS IN PROGRAM MEMORY TOGETHER WITH IMAGINARY ADDRESS INFORMATION
END

Fig.21